CLAIMS

1. A system for decoding video data encoded with a particular standard, said system comprising:

a video decoder for decoding the video data encoded with the particular standard;

instruction memory for storing:

a first set of instructions for decoding encoded video data according to a first encoding standard; and

a second set of instruction for decoding encoded video data according to a second encoding standard;

a host processor for providing an indication to the video decoder indicating the particular encoding standard; and

wherein the video decoder executes the first set of instructions if the indication indicates that the particular encoding standard is the first encoding standard and executes the second set of instructions if the indication indicates that the particular encoding standard is the second encoding standard.

2. The system of claim 1, wherein the first encoding standard comprises MPEG-2 and the second encoding standard comprises MPEG-4.

3. The system of claim 1, wherein the instruction memory stores a third set of instructions for decoding encoded video data according to a third encoding standard, and wherein the video decoder executes the third set of instructions if the indication indicates that the particular encoding standard is the third encoding standard.

4. The system of claim 3, wherein the first encoding standard comprises MPEG-2, the second encoding standard comprises MPEG-4, and the third encoding standard comprises DV-25.

5. The system of claim 3, wherein the instruction memory stores a fourth set of instructions for decoding the video data in accordance with the first encoding standard, the second encoding standard, and the third encoding standard.

6. The system of claim 1, further comprising a register for storing the indication from the host processor.

7. The system of claim 6, wherein the instruction memory stores a fifth set of instructions, wherein execution of the instructions by the host processor cause:

detecting the particular encoding standard; and

writing the indicator to the register.

8. A method for decoding video data encoded with a particular standard, said method comprising:

providing an indication to a video decoder indicating the particular encoding standard to the video decoder;

executing a first set of instructions if the indication indicates that the particular encoding standard is a first encoding standard; and

executing a second set of instructions if the indication indicates that the particular encoding standard is the second encoding standard.

9. The method of claim 8, wherein the first encoding standard comprises MPEG-2 and the second encoding standard comprises MPEG-4.

10. The method of claim 8, further comprising executing the third set of instructions if the indication indicates that the particular encoding standard is the third encoding standard.

11. The method of claim 10, wherein the first encoding standard comprises MPEG-2, the second encoding standard comprises MPEG-4, and the third encoding standard comprises DV-25.

12. The method of claim 10, executing a fourth set of instructions for decoding the video data in accordance with the first encoding standard, the second encoding standard, and the third encoding standard.

13. The method of claim 8, further comprising:

detecting the particular encoding standard; and

writing the indicator to a register.

14. A system for decoding video data encoded with a particular standard, said system comprising:

a code memory for instructions; and

a processor for loading the code memory with a first set of instructions for decoding encoded video data according to a first encoding standard, where the video data is encoded according to the first encoding standard and for loading the code memory a second set of instruction for decoding encoded video data according to a second encoding standard, wherein the video data is encoded according to the second encoding standard.

15. The system of claim 14, wherein the processor loads the code memory after receiving an indication from a host processor indicating the particular encoding standard.

16. The system of claim 14, wherein execution of the first set of instructions by the processor controls a first plurality of circuits, and execution of the second set of instructions controls a second plurality of circuits.

17. The system of claim 14, further comprising a slave engine, said slave engine further comprising:

another instruction memory for storing a third set of instructions if the encoding standard is the second encoding standard.

18. The system of claim 17, wherein the slave engine comprises a third plurality of circuits, wherein the execution of the third set of instructions controls the third plurality of circuits.